	Enrollm	ent No•		Evan	n Seat No:					
	Enrollment No: Exam Seat No: C.U.SHAH UNIVERSITY									
	Winter Examination-2018									
	Subject Name: Computer Organization & Architecture									
	Subject Code: 47		TE04COA1	Branch: B	Branch: B.Tech (CE)					
	Semester	r: 4	Date: 25/10/2018	3 Time: 10:30	0 To 01:30	Marks: 70				
	 Instructions: (1) Use of Programmable calculator & any other electronic instrument is prohibited. (2) Instructions written on main answer book are strictly to be obeyed. (3) Draw neat diagrams and figures (if necessary) at right places. (4) Assume suitable data if needed. 									
Q-1	a) b) c) d) e) f) g) h) i) k) l) m) n)	Define What i What i Define	BUN. Machine level language CDR. s interrupt? SZA. ION. Hardwired control. HLT. IOF. s Subroutine?	sor? ge.			(14)			
Q-2		Attem _y Explain	estions from Q-2 to Q- pt all questions a different types of inst a different types of add	truction.	e example.		(14) (7) (7)			

Atte

Q-2		Attempt all questions	(14)
	(a)	Explain different types of instruction.	(7)
	(b)	Explain different types of address with suitable example.	(7)
Q-3		Attempt all questions	(14)
	(a)	Explain shift micro operation with example.	(7)
	(b)	Write a short note on selective operation.	(7)
Q-4		Attempt all questions	(14)
-	(a)	Explain Instruction Pipeline with proper diagram.	(7)



	(b)	What is Instruction Cycle? Explain Instruction Cycle with proper diagram.	(7)
Q-5		Attempt all questions	(14)
	(a)	Explain ZERO, ONE, TWO, THREE address instruction in details.	(7)
	(b)	Differentiate between superscalar processor and vector processor.	(7)
Q-6		Attempt all questions	(14)
_	(a)	Write a short note on second pass of assembler.	(7)
	(b)	Draw architecture of General Register Organization.	(7)
Q-7		Attempt all questions	(14)
_	(a)	Differentiate between RISC and CISC.	(7)
	(b)	Write a short note on Accumulator unit.	(7)
Q-8		Attempt all questions	(14)
-	(a)	Explain Pipeline Processing using P*Q+R.	(7)
	(b)	Write a short note on bus and memory transfer.	(7)

